Bio

Dr. Jabeom Koo, earned his B.S. and M.S. degrees in 2006 and 2008 respectively from Korea University in South Korea. After graduation, he worked at SK Hynix Semiconductor Inc. in Korea until August 2011, as an Analog Circuit Design Engineer. There, he focused on designing High-speed input/output (I/O) circuit for 512GB Graphic Dynamic Random Access Memory (DRAM) memory chip with 45nm CMOS technology.

Dr. Koo received his Ph.D. degree in Electrical Engineering from the University of Washington, Seattle, in March 2016. He then joined the Analog I/O design team at Intel Corporation in Hillsboro, OR for i5/i7 CPU design. After the first tape-in with CMOS 10nm technology, he moved to the RF technology team in Advanced Design group. He worked as a RF/Analog Circuit Design Engineer and participated in 140GHz Transceiver/Receiver system design for server chips communication. He also had additional responsibilities as a lab manager controlling all measurements for Intel 22nm FinFet technology development. His current research interests are in the area of RF IC design for wireless applications.

He joined Cooper Union at Sept. 2020 as an Assistant Professor in Electrical Engineering deparment. The research topic is low power and low noise RF front-end circuit design with MEMS Resonator for wireless applications such as Zigbee, Bluetooth Low Energy and 6G.

Seminar topic : 300mV Power supply Analog/RF circuit design

WAFER scale high Q MEMS resonators are becoming attractive alternatives to quartz owing to their small size, low cost, and integration potential. RF front-end circuits including oscillators using MEMS resonator have showed superior performance compared to quartz oscillators in terms of phase noise performance. A phase noise is an important performance metric for a reference oscillator as it dominates the in-band phase noise of a frequency synthesizer in a radio. To be more specific, a high data rate in emerging communication systems such as 5G/6G wireless systems, and wireless local area network (WLAN) systems require high bandwidth efficiency. That’s why it is critical to lower the phase noise considering such wireless applications. In addition to the phase noise, the power consumption of the circuits has been bottlenecked for achieving low power receiver or transceiver system.
It is therefore inevitable to design with super low power supply to meet recent wireless application environments and meet stringent specification of phase noise simultaneously. I’d like to address 300mV Power supply circuit design to break through phase noise and power consumption requirements.